Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A system for processing an input signal, the system comprising:

- a signal processing subsystem receiving and processing said input signal and producing a system output signal;

- an adaptive predistortion subsystem receiving at least two internal input signals and producing at least two predistorted signals by applying a deliberate predistortion to said at least two internal input signals;

- a feedback signal processing subsystem for receiving and processing a feedback signal derived from said system output signal; and

- a delay subsystem for providing a delay to a replica of said input signal to produce a delayed signal, said delayed signal being used by said adaptive predistortion subsystem and said feedback processing subsystem,

wherein

- said adaptive predistortion subsystem distorts said input signal to compensate for distortions in said system output signal;

- said signal processing subsystem decomposes said input signal into separate components to produce said at least two internal input signals, each of said separate components being processed separately;

- said processing subsystem combines said predistorted signals after processing to produce said system output signal;

- an output of said feedback processing subsystem is used by said adaptive predistortion subsystem;

- said deliberate predistortion applied to said input signal by said adaptive predistortion subsystem to produce said predistorted signal is adjusted based on said system output signal.

2. (Original) A system according to claim 1 wherein said signal processing subsystem comprises:

- a signal decomposer for decomposing said predistorted signal into at least two components;

- at least two signal component processor blocks, each signal processor block receiving an output of said signal decomposer and each signal processor block separately processes said output received from said signal decomposer; and

- a combiner receiving a processed output from each of said at least two signal component processor blocks, said combiner producing said system output signal from said processed outputs of said at least two signal component processor blocks.

3. (Original) A system according to claim 2 wherein at least one of said at least two signal component processor blocks includes an amplifier.

4. (Original) A system according to claim 3 wherein said amplifier is a non-linear amplifier.

5. (Original) A system according to claim 1 wherein said system is part of a signal transmission system.

6. (Original) A system according to claim 1 wherein at least some of said distortions are due to said combiner.

7. (Original) A system according to claim 3 wherein said amplifier is a switch mode amplifier.

8. (Original) A system according to claim 3 wherein said amplifier has a low output impedance.

9. (Original) A system according to claim 1 wherein said deliberate predistortion adjusts a magnitude of said system output signal by adjusting at least one of said at least two internal signals.

10. (Original) A system according to claim 1 wherein said deliberate predistortion adjusts a phase of said system output signal by adjusting at least one of said at least two internal input signals.

11. (Original) A system according to claim 1 wherein said deliberate predistortion is based on at least one entry in a lookup table.

12. – 18. (Cancelled).

12 ~~19.~~ (Original) A system according to claim 1 wherein said predistortion subsystem receives a replica of said system output signal.

13 ~~20.~~ (Original) A system according to claim 2 wherein said deliberate predistortion is dependent on differences between said input signal and said replica of said system output signal.

PN

14 ~~21.~~ (Original) A system according to claim 11 wherein entries in said lookup table are periodically updated based on characteristics of a replica of said system output signal.

15 ~~22.~~ (Original) A system according to claim 11 wherein said deliberate predistortion is based on an interpolation of entries in said table.

16 ~~23.~~ (Original) A system according to claim 1 wherein said predistortion subsystem includes:

- determining means for determining said deliberate predistortion;
- adjustment means for applying said deliberate predistortion to said input signal;
- update means for periodically updating said determining means based on said system output signal.

17 ~~24.~~ (Original) A system according to claim 16 ~~23~~ wherein said adjustment means receives parameters of said deliberate predistortion from said determining means.

25. – 26. (Cancelled).

18 27. (Currently Amended). An adaptive predistortion subsystem for use with a signal processing system which produces a system output signal, the predistortion subsystem comprising:

-determining means for determining a deliberate predistortion to be applied to an input signal;

- adjustment means for applying said deliberate predistortion to said input signal;

- update means for periodically updating said determining means based on characteristics of said system output signal

wherein said adaptive predistortion subsystem uses

- an output of a delay subsystem for delaying said input signal and

PN

- an output of a feedback processing subsystem for processing a feedback signal derived from said system output signal to determine said deliberate Predistortion and;

wherein said adaptive predistortion subsystem protects against subsystem instability by only updating said determining means in specific predetermined instances.

28. – 31. (Cancelled).

19 32. (Original) A system according to claim 1 wherein said delay subsystem comprises:

- a plurality of delay elements;
- means for sampling said input signal;
- means for storing samples of said input signal;
- means for selecting selected samples of said input signal; and
- means for combining said selected samples of said input signal.

20 33. (Original) A system according to claim 1 wherein said delay subsystem comprises separate subsystems for separately delaying a magnitude and a phase of said input signal.

21 34. (Original) A system according to claim 1 wherein said feedback signal processing subsystem comprises means for adjusting a phase of a replica of said system output signal.

35. – 37. (Cancelled).

(cancelled)

38. (Withdrawn) A method of initializing a phase correction to be applied to a feedback signal, said feedback signal to be used in determining a deliberate predistortion for a signal processing system, the method comprising:

a) initiating a coarse delay search

b) selecting a time window of W samples of said feedback signal and an input signal with a predetermined sample delay increments of δ between samples

c) calculating an inner product P_δ by performing a complex multiply and accumulate process for the W samples in the time window

PN

d) storing a maximum $|P|_\delta$ found

e) repeating steps c) and d) for subsequent time windows and incrementing δ by a predetermined amount for each time window

f) repeating steps b) - e) for a fine delay search using fractional sample increments to cover a predetermined delay range, said delay range being centered on a maximum delay increment δ_{max} found during said coarse delay search.

(cancelled)

39. (Withdrawn) A method according to claim 38 wherein said inner product process is defined by

$$P_\delta = A_{MAC} \cdot \sum_{k=n\cdot W}^{n\cdot W+W-1} \exp(j \cdot (\angle x_\delta(k) - \angle z(k)))$$

where

$\angle x_\delta(k)$ is a phase of said input signal

$\angle z(k)$ is a phase of said feedback signal

A_{MAC} is a constant

~~n is an integer denoting a time window~~

(cancelled)

40. (Withdrawn) A method according to claim 38 ~~wherein said~~ phase correction is a phase of said maximum P_δ.

41. – 44. (Cancelled).

22 ~~45.~~ (Original) A system according to claim 1 wherein said predistorted signal is adjusted based on said system output signal and said input signal.

46. (Cancelled.)

23 ~~47.~~ (Original) A system according to claim ~~23~~ 16 wherein said update means periodically updates said determining means based on said system output signal and said input signal.

(cancelled)

PN. 48. (Withdrawn) A method according to claim 38 wherein said inner product ~~P_δ is based~~ on a phase ~~of said input signal~~ and on a phase of a system output signal.

24 ~~49.~~ (Original) An adaptive predistortion subsystem according to claim ~~27~~ 18 wherein said subsystem is embedded inside said signal processing system such that said input signal is a decomposed component of an input signal to said signal processing system.

25 ~~50.~~ (Original) An adaptive predistortion subsystem according to claim ~~27~~ 18 further including a distortion monitor for monitoring an amount of distortion in said system output signal.

26 ~~51.~~ (Original) An adaptive predistortion subsystem according to claim ~~50~~ 25 wherein said distortion monitor generates an alarm when said distortion exceeds a predetermined level.

52. (Cancelled).

27 53. (Original) An adaptive predistortion subsystem according to claim 18 wherein said subsystem is controlled by a preprogrammed control device.

28 54. (Original) An adaptive predistortion subsystem according to claim 27 wherein said control device is programmed with a predefined set of states, each state having associated with it a predefined set of commands to be executed by said subsystem when said device is in said state.

29 55. (Original) An adaptive predistortion subsystem according to claim 18 wherein said subsystem operates based on a duty cycle such that said subsystem is operating only a function of the time.

30 56. (Original) An adaptive predistortion subsystem according to claim 29 wherein said subsystem is controlled by a preprogrammed control device.

PN

31 57. (Original) An adaptive predistortion subsystem according to claim 30 wherein said duty cycle is determined by said control device.

32 58. (Original) An adaptive predistortion subsystem according to claim 27 wherein said update means updates said determining means based on a duty cycle determined by said control device.

33 59. (Original) An adaptive predistortion subsystem according to claim 27 wherein said subsystem initializes itself based on a duty cycle dependent on a number of updates by which said update means updates said determining means.

34 60. (Original) An adaptive predistortion subsystem according to claim 28 wherein said control device comprises:

- a processor means for receiving and processing data relating to a status of said subsystem;
- a first memory means for storing said data; and
- a second memory means for storing preprogrammed settings for said device.

(cancelled)

61. (Withdrawn) A preprogrammed control device for use in controlling an adaptive predistortion subsystem, said device being programmed with a predefined set of states, each state having associated with it a predefined set of commands to be executed by said subsystem when said device is in said state, the device comprising:

- a processor means for receiving and processing data relating to a status of said subsystem;

- first memory means for storing said data; and

- second memory means for storing preprogrammed settings for said device,

wherein

when said device detects one of a set of specific, predetermined conditions, said device switches from one state to another.

(cancelled)

62. (Withdrawn) A control device according to claim 61 wherein said device controls an update duty cycle for said subsystem, said update duty cycle being determinative of how often said subsystem updates at least one internal lookup table.

(cancelled)

63. (Withdrawn) A control device according to claim 61 wherein said device controls an initialization duty cycle for said subsystem, said initialization duty cycle being determinative of how often said subsystem initializes itself.

(cancelled)

64. (Withdrawn) A control device according to claim 61 wherein said initialization duty cycle is dependent on how often said subsystem updates at least one internal lookup table.

(cancelled)

65. (Withdrawn) A control device according to claim 61 wherein said control device switches from one state to another based on input from a distortion monitor which monitors a level of distortion for said subsystem.

(cancelled)

66. (Withdrawn) A control device according to claim 61 wherein said adaptive predistortion subsystem comprises:

-determining means for determining a deliberate predistortion to be applied to an input signal;

- adjustment means for applying said deliberate predistortion to said input signal;

- update means for periodically updating said determining means based on characteristics of said system output signal

wherein said adaptive predistortion subsystem uses

- an output of a delay subsystem for delaying said input signal and

- an output of a feedback processing subsystem for processing a feedback signal derived from said system output signal to determine said deliberate predistortion.

Cancelled

67. (Withdrawn) A method according to claim 38 wherein said signal processing system comprises

- a signal processing subsystem receiving and processing said input signal and producing a system output signal;

- an adaptive predistortion subsystem receiving at least two internal input signals and producing at least two predistorted signals by applying a deliberate predistortion to said at least two internal input signals;

- a feedback signal processing subsystem for receiving and processing a feedback signal derived from said system output signal; and

- a delay subsystem for providing a delay to a replica of said input signal to produce a delayed signal, said delayed signal being used by said adaptive predistortion subsystem and said feedback processing subsystem,

wherein

- said adaptive predistortion subsystem distorts said input signal to compensate for distortions in said system output signal;

- said signal processing subsystem decomposes said input signal into separate components to produce said at least two internal input signals, each of said separate components being processed separately;

- said processing subsystem combines said predistorted signals after processing to produce said system output signal;

- an output of said feedback processing subsystem is used by said adaptive predistortion subsystem;

- said deliberate predistortion applied to said input signal by said adaptive predistortion subsystem to produce said predistorted signal is adjusted based on said system output signal.

35 ~~68~~. (Original) A system according to claim 1 wherein said adaptive predistortion subsystem distorts said internal input signal based upon which decomposition method is used by said signal processing subsystem to decompose said input signal.

36 ~~69~~. (Original) A system according to claim ~~68~~ 35 wherein said adaptive predistortion subsystem includes multiple lookup tables for use in determining said deliberate predistortion.

37 ~~70~~. (Original) A system according to claim ~~69~~ 36 wherein said adaptive predistortion subsystem determines which lookup table to use in determining said deliberate predistortion based on which decomposition method is used by said signal processing subsystem to decompose said input signal.

PN

38 ~~71~~. (Original) A system according to claim 1 wherein said deliberate predistortion applied to said at least two internal input signals by said adaptive predistortion subsystem to produce said at least two predistorted signals is adjusted based on a signal denoting a decomposition method used by said signal processing subsystem.

39 ~~72~~. (Original) A system according to claim ~~71~~ 38 wherein said decomposition method used by said signal processing subsystem comprises left triangle decomposition or right triangle decomposition.

40 ~~73~~. (Original) A system according to claim ~~70~~ 37 wherein said adaptive predistortion subsystem separately determines for each internal input signal a lookup table to be used in determining said deliberate predistortion.

(cancelled)

74. (Original) A method according to claim 12 further including the step of determining a decomposition method used in decomposing said input signal.

(cancelled)

75. (Original) A method according to claim 74 further including the step of determining said deliberate distortion based on which decomposition method is used in decomposing said input signal.

(cancelled)

76. (Original) A method according to claim 75 further including the step of selecting a lookup table from at least two lookup tables to be used in determining said deliberate distortion based on which decomposition method is used.

(cancelled)

77. (Original) A method according to claim 74 wherein said decomposition method is selected from a group comprising left triangle decomposition and right triangle decomposition.